A Custom Interposer for Wire-Free Electrical Contact to Air-Sensitive 2D Heterostructures

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PROJECT RECORD
Work carried out 2022; unpublished. Interposer and boards built and a test device made; validation not carried through. No transport data are reported here.

AIR-SENSITIVE TWO-DIMENSIONAL CRYSTALS SUCH AS BLACK PHOSPHORUS AND $NbSe_2$ MUST BE exfoliated, stacked, contacted and cooled without exposure to the atmosphere. Wire bonding, the established route to electrical contact, is manual, single-use and difficult inside a glovebox, and the usual alternative, hBN encapsulation, modifies the system under study. We describe a low-profile compression interposer that eliminates the wire bond: twenty signal channels are carried by captive gold-plated beryllium-copper "fuzz button" contact pins that press directly on lithographically defined pads on the device chip, so mounting a device requires only seating the die in a pocket and tightening four screws. A two-step lithography process fixes a single bond-pad footprint for all devices despite the irregular geometry of exfoliated flakes. The hardware was built; quantised-transport validation was not completed and no transport data are reported.

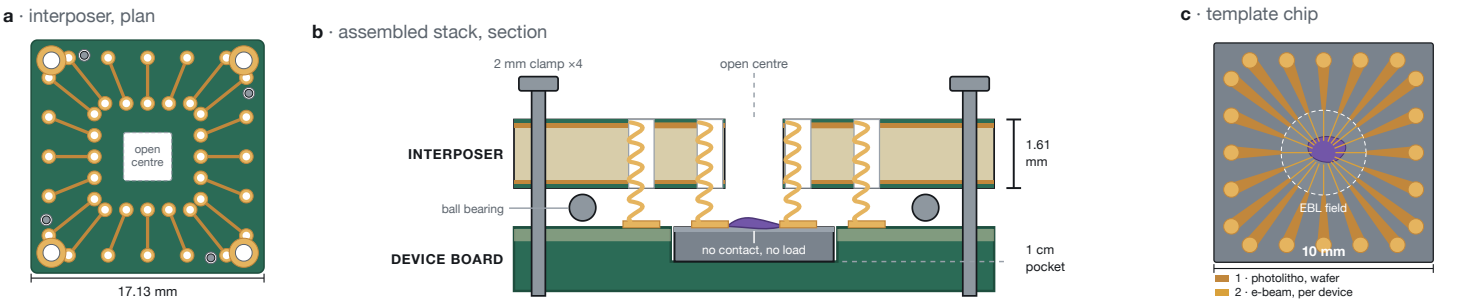


Fig. 1. (a) Forty vias form an inner ring landing on the chip and an outer ring landing on the carrier board, paired by copper traces into 20 channels. Corner holes take the clamping screws; four smaller seats hold ball bearings for alignment. **(b)** The die sits in the pocket with its top face flush to the board. Nothing touches the active area, so clamping puts no strain on the device. **(c)** Bond pads and coarse traces are patterned once at wafer scale; only the fine leads inside the e-beam field are written per device.

1 INTRODUCTION

Two-dimensional materials have been studied intensively for two decades for electronic and optical properties that survive to the single-layer limit, and for the devices made by stacking them.[1] Several of the most studied crystals are unstable in air: few-layer black phosphorus takes up moisture and swells by more than 200 %, and ambient exposure etches flakes layer by layer until devices fail within days.[2] Fabrication in an inert atmosphere is by now well developed: complete cleanroom workflows have been moved into gloveboxes,[3] which also limits organic contamination. Making electrical contact to these devices remains a problem. Wire bonding is manual and difficult through glovebox gloves; each bond is single-use, so reusing a carrier board means de-bonding a working device; and the finished bond is a delicate wire that must survive transfer to a cryostat.

The common workaround is to encapsulate the flake between layers of chemically inert hexagonal boron nitride.[4] Encapsulation protects the material but is not innocuous: graphene nearly aligned to hBN develops a moiré superlattice that reconstructs its band structure,[5] and the strain introduced by stacking shifts electronic properties in MoS_2.[6] For a measurement of the intrinsic response of a bare crystal, encapsulation is not an option.

The semiconductor industry faces a related problem in device test and addresses it with flip-chip bonding and probe cards: reusable hardware with a defined contact pattern that serves many devices. Compression interposers already appear in cryogenic qubit packaging,[7] where they join two circuit boards and the final connection to the chip is still wire bonded. Here the pins land directly on the device chip, so a device can be electrically connected entirely within an inert environment.

2 INTERPOSER

The interposer is a two-layer board: a nominal 60 mil FR4 core between 1.4 mil layers of 1 oz copper, each under 1 mil of solder resist, 17.13 mm square and 1.61 mm thick. Forty 24 mil holes are drilled in two rings and paired by traces, giving five signal channels per side, twenty in total. Each hole holds a captive contact pin: a single strand of Au/BeCu wire wound into a taut helical coil, which compresses when the boards are clamped and makes electrical contact between the board and pre-defined pads on the chip. The pin diameter ordered was not recorded; the nearest catalogue size, 0.020 in., seats in a 0.0220–0.0225 in. hole and is rated 5 A continuous, compliant over 15–30 % of its length, usable on 0.8 mm pitch, with 10–20 mΩ contact resistance depending on source.[8] Contacts of this type have operated from room temperature to millikelvin over several hundred compression cycles in dilution refrigerators.[7] Because each pin is an independent spring, the array accommodates any height mismatch between a diced chip and the surrounding board without lapping or shimming (Appendix A.1).

AS-BUILT SPECIFICATION

Outline / thickness	17.13 mm sq. / 1.61 mm
Construction	2-layer, 60 mil FR4 core, 1 oz Cu
Vias	40 × 24 mil (0.61 mm)
Signal channels	20 (5 per side)
Contact pins	captive Au/BeCu coil
Clamp / registration	4 × 2 mm screw, 4 × 1.134 mm ball
Device pocket	1 cm², chip flush to board

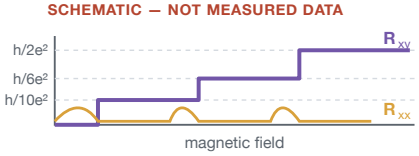
The die rests in a 1 cm² pocket in the carrier board, top face flush with the surface; the interposer is placed on top, and four 2 mm corner screws draw the stack together, providing the contact force, a galvanic connection between the boards, and alignment. Ball bearings in smaller holes beside the screws align the boards more tightly. The centre of the interposer is removed, which keeps the device optically accessible *in situ*; and since the interposer never touches the active area, clamping introduces no strain there.

3 TEMPLATE CHIP

Exfoliated flakes are irregular, so the fine leads that reach them must be written for each device by electron-beam lithography; the millimetre-scale pads and traces that reach the interposer are the same for every device and would only add write time. The pattern is therefore split by length scale. The bond-pad ring and coarse traces are patterned once by photolithography across a 6″ silicon wafer, which is then diced into template chips. A device is assembled on a template chip, and electron-beam lithography writes only the short fine leads from the flake to the inner ends of the coarse traces. Bond-pad placement is standardised across materials without increasing the write time, and because the coarse traces terminate close to the die edge, the number of available connections is increased.

4 QUANTUM HALL MEASUREMENTS

The interposer was tested with a Hall bar with gold contacts on monolayer graphene. The quantum Hall effect is a suitable benchmark because the measured quantities are absolute and four-terminal: plateaus occur at $R_{xy} = h/ve^2$ with $\nu = \pm 2, \pm 6, \pm 10$ in monolayer graphene[9,10] ($h/e^2 = 25.813$ kΩ, so 12.906 kΩ at $\nu = 2$), values set by fundamental constants rather than by the interconnect. Series resistance in the pins drops out of a four-terminal measurement, while intermittency, failure under thermal cycling, or crosstalk would appear as noise on the plateaus or as their absence (Appendix A.3).



Expected quantum Hall signature, drawn schematically. Not measured data.

Status. The interposer and carrier boards were fabricated and the graphene Hall bar was made and mounted, but the measurement was not carried to a quantised-transport data set before the project ended; no transport results are reported here. The electrical figures quoted above are supplier and literature values for this class of contact, not measurements of this hardware.

5 FUTURE WORK

Four measurements would complete the validation. (i) Quantised transport through the interposer: R_{xy} and R_{xx} against field at 4 K and at base temperature, compared against the same die wire-bonded conventionally. (ii) Contact metrology: per-channel resistance in the compressed state at millikelvin and its drift over thermal cycles, which supplier data cannot settle. (iii) The intended application: an unencapsulated air-sensitive flake, black phosphorus or $NbSe_2$, assembled, mounted and sealed entirely inside a glovebox, measured against an encapsulated control. (iv) Channel count and bandwidth: at the 0.8 mm pitch limit the footprint is far from saturated (a comparable interposer for a 17.4 × 19.5 mm device board carries 88 contacts on 0.38 mm holes[7]), so twenty channels is a conservative first iteration; a higher count requires smaller pins and a measured alignment budget. The pins are specified to Ka/Q band[8] and a comparable interposer does not limit signal fidelity below 20 GHz,[7] but a two-layer FR4 board will; radio-frequency use requires a low-loss laminate.

[1] X. Liu and M. C. Hersam, Nat. Rev. Mater. **4**, 669 (2019).
[2] J. O. Island *et al.*, 2D Mater. **2**, 011002 (2015).
[3] M. J. Gray *et al.*, Rev. Sci. Instrum. **91**, 073909 (2020).
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[5] B. Hunt *et al.*, Science **340**, 1427 (2013).
[6] X. Han *et al.*, J. Phys. Chem. C **123**, 14797 (2019).
[7] J. I. Colless and D. J. Reilly, Rev. Sci. Instrum. **85**, 114706 (2014).
[8] Custom Interconnects, *Fuzz Button technical data* (0.020 in.); Cinch data differ.
[9] K. S. Novoselov *et al.*, Nature **438**, 197 (2005).
[10] Y. Zhang *et al.*, Nature **438**, 201 (2005).

Appendix · Mechanical and thermal budget

This appendix estimates the mechanical and thermal margins of the design in Fig. 1: whether the clamped contact survives cooldown (A.1), the load the pins place on the bond pads (A.2), what the quantum Hall measurement can establish (A.3), and how the device thermalises (A.4). Every figure is quoted from the cited source or computed from it as shown. Where the main text does not fix a parameter (carrier thickness, screw alloy, pin diameter) a standard value is assumed and marked in place; the measurements of §5 are the corresponding experimental checks.

A.1 THERMAL CONTRACTION AND CONTACT FORCE

Contact is maintained only if the pins remain compressed on cooling from 293 K to base temperature. Integrated thermal contraction to 4 K, from the NIST curve fits[11] (G-10 CR is the standard cryogenic analogue of FR4; the fits terminate at 10–12 K, below which the expansion coefficient is negligible):

G-10, normal (through-thickness)	0.714 %
G-10, warp (in-plane)	0.240 %
304 stainless	0.297 %
silicon	0.022 %

The clamp path is the interposer plus a carrier board of standard 1.6 mm thickness, 3.2 mm of G-10: the boards contract through their thickness by 22.9 μm and the screws (assumed stainless) by 9.5 μm, so the joint loses **13.4 μm** of compression. A pin is no shorter than the 1.61 mm board it seats in, so its nominal 20 % compliance corresponds to at least 320 μm of travel;[8] cooling therefore consumes about 4 % of the working range, a margin of **24×**. In plane, a pad at the edge of the 10 mm die lies 5 mm from centre: the via above it moves 12.0 μm and the silicon pad 1.1 μm, a differential of 10.9 μm, about 2 % of the 508 μm pin diameter. A rigid contact, by comparison, would open by 13 μm on the first cooldown.

A.2 LOAD ON THE BOND PAD

The suppliers quote 34–71 g per pin;[8] spread over a 0.020 in. face this is a nominal pressure of **1.7–3.4 MPa**. A wafer probe applies less force, 0.5–15 g per probe being ordinary practice,[13] but through a tip small enough to fit a 50–100 μm pad pitch,[12] so 5–10 g on a 10–20 μm tip corresponds to a few hundred MPa, two orders of magnitude above these pins, and is routine on soft aluminium pads. Probe-mark damage is moreover dominated by lateral scrub and punch-through, and a gold-plated pin on a gold pad requires no scrub to break an oxide layer. The arithmetic does not settle everything: a wound-wire pin makes contact at discrete asperities, so the local pressure exceeds the nominal figure, and pad condition after repeated mating must be established by inspection, which was not carried out.

A.3 SCOPE OF THE QUANTUM HALL TEST

The BIPM guidelines for reliable measurement of the quantised Hall resistance require voltage-contact resistances below 100 Ω on the $\nu = 2$ plateau and below 10 Ω on $\nu = 4$, with current contacts in the mΩ range.[14] At 10–20 mΩ these pins sit three to four orders of magnitude inside the $\nu = 2$ tolerance. Observation of the plateaus therefore establishes that the link is present and stable, but it is not a measure of contact quality: a contact could degrade a thousandfold before the quantisation was affected. Contact resistance must be measured directly, by the two-, three- and four-terminal procedures specified in the same document,[14] which is why it appears as a separate item of future work.

A.4 THERMALIZATION

Electrons in the device thermalise mainly through the leads, so the contact must conduct heat as well as signal. Taking the Sommerfeld value $L_0 = 2.44 \times 10^{-8}\ \mathrm{W\Omega K^{-2}}$, the Wiedemann–Franz thermal conductance of a single 20 mΩ contact, L_0T/R, is 122 nW/K at 100 mK and 12 nW/K at 10 mK; the contact itself is not the limiting thermal link. The interposer provides no filtering, however, and filtering together with thermal anchoring is what limits the electron temperature in practice: an optimised setup reaches 28 ± 2 mK at an 18 mK bath temperature.[15] In the comparable system of ref. 7 the RC filters (10 kΩ, 15 nF, $f_c \approx 1$ kHz) are placed on the signal board beneath the interposer,[7] the natural location here as well.

[11] NIST Cryogenic Material Properties Database, trc.nist.gov/cryogenics (G-10 CR, 304 stainless, silicon linear expansion).

[12] O. Weeden, *Probe Card Tutorial*, Keithley Instruments.

[13] Venture Mfg., *What Is a Probe Card* (contact force 0.5–15 g per probe).

[14] BIPM, *Revised technical guidelines for reliable DC measurements of the quantized Hall resistance*.

[15] J. van der Heijden, *Electron thermometry*, arXiv:2403.16305 (2024).